AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated hereafter.

Claims:

1. (Currently Amended) A method for generating a set of test ~~sequenceevectors~~ for testing an integrated circuit, each test ~~sequenceevector~~ of the set of test ~~sequenceevectors~~ containing a plurality of bits defining test inputs for the integrated circuit, the method comprising the steps of:

defining a list of faults for the integrated circuit;

generating at least one test ~~sequenceevector~~ that defines values for those inputs necessary to detect at least one target fault selected from the list of faults, the values comprising only a portion of the bits of the at least one test ~~sequenceevector~~, wherein a remainder of the bits in the at least one test ~~sequenceevector~~ are unspecified bit positions; and

setting the values of a plurality of the unspecified bit positions using a non-random filling methodology.

2. (Original) The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions to a value of one.

3. (Original) The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions to a value of zero.

4. (Original) The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes extending a value of a last specified bit position to set a plurality of the unspecified bit positions to a value equal to the last specified bit position.

5. (Original) The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions using a repeating pattern of ones and zeros.

6. (Original) The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions using an algorithm that is conducive to compression.

7. (Original) The method as defined in claim 1, further including the step of setting a plurality of the unspecified bit positions in accordance with a random filling methodology.

8. (Currently Amended) The method as defined in claim 1, further including the steps of:

adding a first test ~~sequenee~~vector to a list of test ~~sequenee~~vectors and marking the selected fault as detected;

generating an additional test ~~sequenee~~vector which defines values for those inputs necessary to detected a target fault selected from the list of faults, and other than one marked as detected;

determining whether the additional test ~~sequenee~~vector may be compacted with any test ~~sequenee~~vector in the list of test ~~sequenee~~vectors, and if so, compacting the additional test ~~sequenee~~vector with a test ~~sequenee~~vector in the set of test ~~sequenee~~vectors, and if not, adding the additional test ~~sequenee~~vector to the set of test ~~sequenee~~vectors.

9. (Currently Amended) The method as defined in claim 1, wherein a first test ~~sequenee~~vector of the plurality of test ~~sequenee~~vectors defines values for those inputs necessary to detect a plurality of target faults selected from the list of faults.

10. (Currently Amended) The method as defined in claim 1, wherein additional test ~~sequenee~~vectors of the plurality of test ~~sequenee~~vectors define values for those inputs necessary to detect a plurality of target faults selected from the list of faults.

11. (Currently Amended) The method as defined in claim 1, wherein a first test ~~sequenceevector~~ of the plurality of test ~~sequenceevectors~~ defines values for only those inputs necessary to detect a target fault selected from the list of faults.

12. (Currently Amended) The method as defined in claim 1, further including the step of fault simulating a first test ~~sequenceevector~~ created in the generating step ~~(b)~~ to determine if the first test ~~sequenceevector~~ detects additional faults, and if so, marking said additional faults as detected.

13. (Original) The method as defined in claim 1, wherein the integrated circuit is a portion of a larger integrated circuit chip.

14. (Currently Amended) The method as defined in claim 1, wherein outputs for the at least one test ~~sequenceevector~~ are generated in response to the compacted condition.

15. (Currently Amended) An apparatus for generating a set of test ~~sequence~~vectors comprising:

first means for evaluating a list of faults and generating at least one test ~~sequence~~vector configured to test at least one fault on the list of faults, the at least one test ~~sequence~~vector defining values for those inputs necessary to detect at least one target fault selected from the list of faults, the values comprising only a portion of the bits of the at least one test ~~sequence~~vector, wherein a remainder of the bits in the at least one test ~~sequence~~vector are unspecified bit positions; and

second means for setting a plurality of the values of the unspecified bit positions using a non-random filling methodology.

16. (Currently Amended) The ~~method~~apparatus as defined in claim 15, wherein the second means sets the values of the unspecified bit positions by setting each of the unspecified bit positions to a value of one.

17. (Currently Amended) The ~~method~~apparatus as defined in claim 15, wherein the second means sets the values of the unspecified bit positions by setting each of the unspecified bit positions to a value of zero.

18. (Currently Amended) The ~~method~~apparatus as defined in claim 15, wherein the second means sets the values of the unspecified bit positions by setting each of the unspecified bit positions to a repeating pattern of ones and zeros.

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19. (Currently Amended) The ~~method~~apparatus as defined in claim 15, wherein the step of setting the values of the unspecified bit positions includes extending a value of a last specified bit position to set a plurality of the unspecified bit positions to a value equal to the last specified bit position.

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20. (Currently Amended) The ~~method~~apparatus as defined in claim 15, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions using an algorithm that is conducive to compression.